Remarks

I. Status of the Claims

In the Office Action dated September 11, 2002, the Examiner: (i) rejected claims 2 and 7 under §112 as being indefinite; (ii) rejected claims 1-6 under §101 as claiming the same invention as that in claims 1-22 of U.S. Patent No. 6,271,686 to Tran et al ("Tran"); (iii) rejected claims 1-3 under §102(e) as being anticipated by U.S. Patent No. 6,201,425 to Kartschoke et al. ("Kartschoke"); and (iv) indicated that claims 7 and 8-16 are allowable over the prior art of record.

In this response, Applicant has amended claims 1-7 and has added new claims 17-21. Claims 1-21 are now pending.

II. Rejection of claims 2-7 under §112

The Examiner rejected claims 2-7 as being indefinite because it was unclear to what structure various elements corresponded. In response, Applicants have: (i) amended claim 2 to clarify that the first and second signals are applied to the gate and drain of the SOI device; (ii) amended claim 6 to clarify that the active discharging device provides a conduction path between the intermediate node and a voltage source; and (iii) amended claim 7 to clarify to replace "a discharge potential" with "a voltage source," and to clarify to what the "intermediate node" refers.

III. Rejection of claims 1-6 under §101

The Examiner rejected claims 1-6 as claiming the same invention as that of claims 1-22 of Tran. Applicant respectively traverses. A statutory type double patenting rejection is not appropriate when one set of claims can be literally infringed without literally infringing a corresponding claim(s) in the other set. *See MPEP §804(II)(A).* In this case, claims 1-16 of Tran include a number of limitations not found in claims 1-6 of the present application, including: "providing a plurality of stacks connected in parallel with one another and between said shared node and a common discharge . . . wherein the plurality of stacks are arranged so as to eliminate any parasitic bipolar transistor current leakage path " (claims 1-16) and "providing a stack

expansion of a plurality of said SOI devices" (claims 17-22). Because claims 1-6 of the present application can be infringed without infringing claims 1-22 of Tran, Applicant respectively submits that it is not claiming the same invention.

IV. Rejection of Claims 1-3 under 35 U.S.C. §102(e)

The Examiner rejected claims 1-3 under §102(e) as being anticipated by Kartschoke. Claims 2-3 are dependent on claim 1 and include all of its limitations. Accordingly, claims 2-3 are not anticipated by Kartschoke if claim 1 is not anticipated by Kartschoke. Applicant respectively asserts that claim 1, as amended, is not anticipated by Kartschoke at least because Kartschoke does not disclose "controlling the conduction of an active discharging device with the input signal."

The invention in claim 1, as amended, is directed at a method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) device located in a logic circuit. The logic circuit in claim 1 is adapted to receive an "input signal" and a "clock signal." The present invention deactivates the parasitic bipolar transistor by controlling the conduction of an active discharging device with the input signal.

Kartschoke, in contrast, describes a top clock stacked circuit that eliminates both charge sharing and deleterious bipolar effect. The top clock stacked circuit in its Fig. 5 comprises a pre-charge PFET 503 and a pre-discharge NFET 505. The pre-charge PFET 503 has a source coupled to V_{DD}, a drain coupled to the first node 111, and a gate that serves as a CLK input. The pre-discharge NFET 505 has a source coupled to ground, a drain coupled to the second node 115 and a gate that serves as an inverse clock (CLK_NOT) input. *Kartschoke, Col. 6, lines 26-40.*

Unlike the invention in claim 1, as amended, the pre-charge PFET and the pre-discharge NFET in Kartschoke are both controlled by a clock-related signal (i.e., CLK or CLK_NOT). Thus, Kartschoke does not disclose "controlling the conduction of an active discharging device with the input signal." For at least this reason, Applicant respectively submits that claims 1-3, as amended, are not anticipated by Kartschoke.

V. Miscellaneous

Applicant has added new claims 17-21 to better protect the invention in the marketplace. Applicant has also amended claims 1-7 to correct minor errors and to more clearly define the invention.

VI. Conclusion

In view of the foregoing comments and amendments, the Applicant respectfully submits that all of the pending claims are in condition for allowance and that the application should be passed to issue.

Respectfully submitted,

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Version with Markings to Show Changes Made

1. (Amended) A method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) device located in a logic circuit, said logic circuit being adapted to receive an input signal and a clock signal, the method comprising:

[C]controlling the conduction of an active discharging device with the input signal, said active discharging device being coupled to an intermediate node of said [SOI device] logic circuit, whereby the parasitic bipolar transistor is deactivated.

2. (Amended) The method of claim 1 [further comprising], wherein the SOI device comprises a gate and a drain, and wherein the method further comprises:

providing a first signal to [a first node] said gate of said SOI device;

providing a second signal to [an input] said drain of said SOI device; and

activating the conduction of said active discharging device according to the state of said first signal [and second signals].

3. (Amended) The method of claim 2 wherein the first signal is [a clock signal] said input signal.

4. (Amended) The method of claim [3] 2 wherein said [first node is charged high] first signal causes said SOI device to conduct current whenever said [clock signal is active low] logic circuit is being pre-charged.

5. (Amended) The method of claim 2 wherein the second signal [is an active low signal applied to said input] pre-charges said drain during a pre-charge cycle.

6. (Amended) The method according to claim 1, wherein the active discharging device provides a conduction path between said intermediate [second] node [of SOI device] and a [common node] voltage source.

7. (Amended) A method of eliminating parasitic bipolar transistor action in a Silicon on Insulator (SOI) Metal Oxide Semiconductor (MOS) dynamic logic circuit having an input, an output, a clock, an active discharge transistor, and a plurality of stacked SOI Metal Oxide Semiconductor (MOS) transistors interconnected to [perform a predetermined logic function defining] define a common node and an intermediate node, wherein:

said plurality of stacked SOI MOS transistors [being] is controlled by a [respective] plurality of inputs[,];

said common node [being] is coupled to a pre-charging device; [and]

said intermediate node [being] is in a path between said common node and a [discharge potential] voltage source, said path defined by said plurality of stacked SOI MOS transistors[,];

said intermediate node [being] is coupled to said common node by at least a first of said plurality of stacked SOI MOS transistors[,]; and

[said intermediate node being coupled to said discharge potential by at least a second of said plurality of stacked SOI MOS transistors, and]

[an] said active discharging transistor is controlled by at least one of said plurality of inputs, said active discharging transistor defining a discharge path between said intermediate node and said [discharge potential] voltage source,

the method comprising:

controlling the conduction of said active discharging transistor during a pre-charge cycle; and

actively discharging said intermediate node[s of the SOI stacked transistors], whereby the parasitic bipolar transistors are deactivated and the charge at said [common] intermediate node is maintained at a predetermined level.

8. (Unchanged) The method according to claim 7, wherein pre-charging occurs during a low state of said clock

9. (Unchanged) The method according to claim 7, wherein pre-charging occurs during a high state of said clock.

10. (Unchanged) The method according to claim 7, wherein during the pre-charging all said inputs are set to a predetermined logic state.

11. (Unchanged) The method according to claim 10, wherein said logic state is low.

12. (Unchanged) The method according to claim 10, wherein said logic state is high.

13. (Unchanged) The method according to claim 7, wherein the step of actively discharging said intermediate nodes prevents the body voltages of said stacked SOI transistors from reaching a voltage stage sufficient to activate the parasitic bipolar transistors of said stacked SOI transistors.

14. (Unchanged) The method according to claim 7, wherein said stacked transistors are N-Field Effect Transistors (NFET) and said active discharging transistors are P-Field Effect Transistors (PFET).

15. (Unchanged) The method according to claim 7, wherein said stacked transistors are P-Field Effect Transistors (PFET) and said active precharging transistors are N-Field Effect Transistors (NFET).

16. (Unchanged) The method according to claim 7, wherein said pre-charging device comprises transistors coupled to said stacked transistors.

17. (New) A method of reducing the effects of parasitic bipolar transistor action in a silicon-on-insulator (SOI) logic circuit during a pre-charge cycle, comprising:

coupling an active discharge device to an intermediate node of the SOI logic circuit; and

controlling the conduction of the active discharging device using a non-clock signal, whereby the charge at the intermediate node is maintained at a predetermined level during the pre-charge cycle.

18. (New) The method of claim 17, wherein the predetermined level is a common ground potential for the SOI logic circuit.

19. (New) The method of claim 17, wherein the non-clock signal comprises an active low signal applied to an input of the SOI logic circuit during the pre-charge cycle.

20. (New) The method of claim 1, wherein said input signal is a non-clock signal.

21. (New) The method of claim 6, wherein the voltage source comprises a system ground.